

Manufacturing with DUV lithography

by S. J. Holmes
P. H. Mitchell
M. C. Hakey

Deep-UV (DUV) lithography has been developed to scale minimum feature sizes of devices on semiconductor chips to sub-half-micron dimensions. This paper reviews early manufacturing experiences at the IBM Microelectronics Division with deep ultraviolet (DUV) lithography at a 248-nm wavelength. Critical steps in the processing of 1Mb DRAM, 16Mb DRAM, and logic gate conductors in devices are discussed. The evolution of DUV lithography tools is also briefly reviewed.

Introduction: Lithographic scaling

Lithographic scaling has historically been accomplished by optimizing the parameters in the Rayleigh model for image resolution: In this model, image resolution = $k_1 \lambda / NA$, and depth of focus (DOF) = $k_2 \lambda / NA^2$, where λ = exposure wavelength and NA = numerical aperture (k_1, k_2 = constants for a specific lithographic process). To pattern devices with decreasing feature sizes, photoresist exposure wavelengths were reduced and numerical apertures were increased.

During the last ten years, image resolution was sufficiently increased to scale minimum dimensions from 1- μm feature sizes for the 1Mb DRAM devices to 0.25- μm features for the 256Mb DRAM. The depth of focus is proportional to the inverse of the square of the numerical aperture; thus, if resolution is enhanced by increasing NA, the depth of focus becomes very small. If the resolution is enhanced by decreasing the wavelength, the corresponding decrease in depth of focus is less severe. As shown in

Figure 1, for lithography at the diffraction limit, a shorter wavelength provides more depth of focus at a particular resolution value because the shorter wavelength allows a lower-NA photolithography tool to achieve equivalent resolution.

The IBM Microelectronics Division has been active in the evolution of lithography throughout the development of the semiconductor industry (**Figure 2**). DRAM production of 64Kb devices utilized scanning exposure equipment operating at a G-line wavelength of 436 nm. These tools were capable of operating at several different exposure wavelengths, including 436 nm, 313 nm, and 245 nm [1]. IBM used these tools for 256Kb DRAM chips by formulating a resist, TNS, which was functional at the 313-nm exposure region [2], allowing the critical feature size to be scaled from 2 μm to 1.4 μm . This approach was repeated for 1Mb DRAM chips, and a 245-nm exposure region was used to obtain the 1- μm critical features with the same tool set, which required the development of the first production deep-UV (DUV) chemically amplified, negative-tone resist [3]. At this time, G-line steppers were introduced at a NA of 0.35, and the process for the production of 1Mb DRAM reverted to G-line lithography. For the 4Mb DRAM generation, stepper technology was extended by scaling the wavelength to the I-line (λ = 365 nm). High-NA (0.42–0.45) G-line steppers were used to manufacture 4Mb pilot line products at 0.8- μm ground rules, while lower-NA (0.35) I-line steppers were used for final qualification of products with 0.6–0.7- μm critical features. For the 16Mb generation, DUV in the 245-nm exposure region was utilized for development and initial production, while very high NA (0.5–0.6) I-line (365 nm)

©Copyright 1997 by International Business Machines Corporation. Copying in printed form for private use is permitted without payment of royalty provided that (1) each reproduction is done without alteration and (2) the *Journal* reference and IBM copyright notice are included on the first page. The title and abstract, but no other portions, of this paper may be copied or distributed royalty free without further permission by computer-based and other information-service systems. Permission to republish any other portion of this paper must be obtained from the Editor.

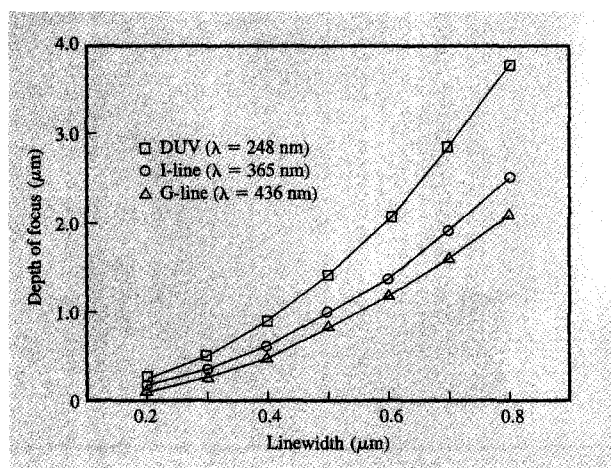


Figure 1

Depth of focus as a function of image resolution, as calculated with the Rayleigh model. Numerical aperture is variable, and increases as resolution increases. For this calculation, $k_1 = k_2 = 0.7$.

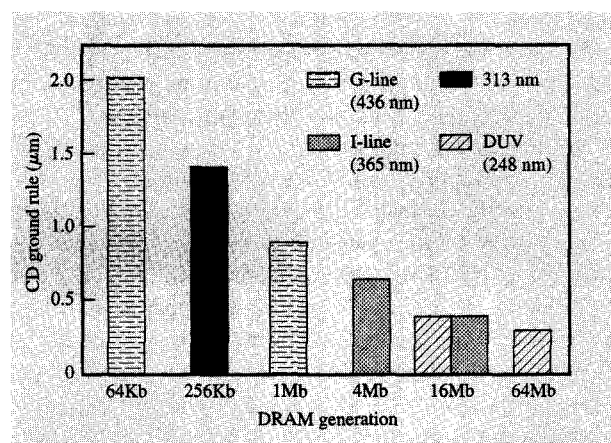


Figure 2

DRAM critical dimension (CD) scaling experience at IBM, detailing minimum-feature-size ground rules and lithographic exposure technology for each DRAM generation. The 16Mb DRAM development and early production used DUV ($\lambda = 248$ nm) lithography; exposure at $\lambda = 365$ nm (I-line) was used for large-volume production.

was used for volume production at 0.4–0.5- μ m image sizes. The 64Mb and 256Mb DRAM generations use high-NA (0.5–0.6) DUV tools at $\lambda = 248$ nm for images at 0.25–0.35- μ m resolution.

During this scaling process, several DUV resist materials were developed and utilized by IBM. While

I-line resists were composed of modified G-line materials, the DUV resists operated by a different mechanism. The DUV region of the mercury arc lamp is of relatively low intensity compared to the I-line and G-line regions. To compensate for low DUV exposure intensities, a chemical amplification method [4, 5] was used to enhance the speed of the DUV resist. This catalytic amplification process, combined with new resins that were less absorbing at $\lambda = 245$ nm than the traditional novolak materials, introduced significantly different resist processing requirements for DUV lithography. These unique process requirements were characterized and included as part of the process of implementing DUV lithography in product applications.

DUV processing for product applications

• 1Mb DRAM: 1985–1986

DUV resist was used at $\lambda = 245$ nm to print the first level of the 1Mb DRAM, which was recessed oxide (Rox) isolation [5]. This level required the printing of a 1- μ m resist spacing between features on a 100-nm silicon nitride film. The image was transferred into the nitride film with an RIE process. DUV was used on this level because the initial G-line steppers were limited to a resolution of 1.2 μ m, and insufficient wafer stage control was available to establish a uniform grid at the first mask level. The scanning exposure tools, which were commonly available in manufacturing areas at that time, were capable of 1- μ m feature resolution at DUV exposure wavelengths ($\lambda = 240$ –250 nm). Since these tools were full-wafer scanners, the first level was printed as a regular grid, with the relative positioning of each chip predominantly established by the reticle fabrication tool. Product overlay could be achieved within the required tolerance by using this regular and repeatable first level as a reference point for the alignment of subsequent mask levels.

The initial DUV resist formulation was a negative-tone material with a new resin, solubility inhibitor, photoactive compound, and developer solution compared to the previously utilized mid-UV resists. The resin was a para-hydroxy-styrene polymer (PHOST) modified with a tertiary-butoxy-carbonyl (tBOC) functionality to impart insolubility in polar solvents and aqueous-base solutions. A sulfonium salt was used as a photo-acid generator, and a post-exposure bake was used to cause a catalytic cleavage of the tBOC group from the exposed resist (Figure 3) [4, 6]. Development in anisole of the exposed and baked resist selectively removed the unexposed material, providing a negative-tone image.

This resist was very sensitive, requiring a 1–5-mJ/cm² exposure dose, depending on the formulation and process conditions. Contrast was high, with a γ value of 8–10, and the 1- μ m resolution requirement of this product

application was easily achieved. With this system, throughput levels of 100 wafers per hour could be achieved with existing scanning exposure equipment. However, a number of difficulties with this system soon became apparent as product application work progressed. While resist adhesion was acceptable on silicon wafers, poor adhesion was obtained on the silicon nitride product film. The hexamethyldisilazane (HMDS) adhesion priming operation, which was effective for conventional development of resists in aqueous solutions, was ineffective for the hydrophobic solvent used in this DUV develop process. Thermal oxidation at the nitride surface to form a silicon oxynitride surface improved resist adhesion sufficiently to warrant further product development.

Metallic oxide residues were identified in the resist stripping baths and traced to the photosensitizer materials used in the DUV resist. These residues were reduced by specifying smaller wafer batches between bath changes and, ultimately, by replacing the metallic components in the resist formulation with organic materials.

Attention also focused on control of the post-exposure bake process, because this parameter became more important for linewidth control than exposure dose levels in the photolithography tool (Figure 4). The catalytic chemical amplification reaction which produced the high resist sensitivity needed for operation at the low light intensities available in DUV was exponentially dependent on the bake temperature used to induce the catalysis. As a result, resist sensitivity also became exponentially dependent on the bake temperature [7].

Not only was the catalytic amplification process of this resist dependent on the bake conditions, but it could also be affected by the presence of contaminants from chemicals in the manufacturing environment. It was observed that freshly coated wafers, when placed in a cassette on the photolithography tool and exposed in sequence, often displayed a continuous shift in linewidth from wafer to wafer across the cassette. The resist steadily became one to three times less sensitive as the delay time from application of resist to its exposure increased. After two to three hours, the resist stabilized at a lower sensitivity value (Figure 5). This behavior was caused by the absorption of chemical bases, such as N-methylpyrrolidone (NMP), into the resist at part-per-billion levels, which interrupted the catalytic image formation process [8] and caused a large change in resist sensitivity. Initially, wafers were deliberately allowed to stand in the manufacturing environment and absorb the chemical contaminants. The resist sensitivity became relatively stable and then could be processed with acceptable linewidth control after the contaminants were absorbed. Because of variations in the manufacturing environment, however, significant shifts in resist sensitivity were

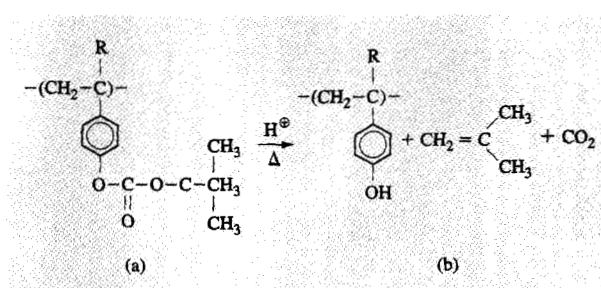


Figure 3

Chemical amplification mechanism for early embodiments of DUV resist. The unexposed resin (a) dissolves in nonpolar solvents, while the exposed and baked resist (b) dissolves in polar solvents. As shown in the chemical reaction, acid, which is generated (from a photoactive sulfonium salt) during exposure, catalytically cleaves the solubility inhibitor from the resin (a) during a post-exposure bake (PEB) process.

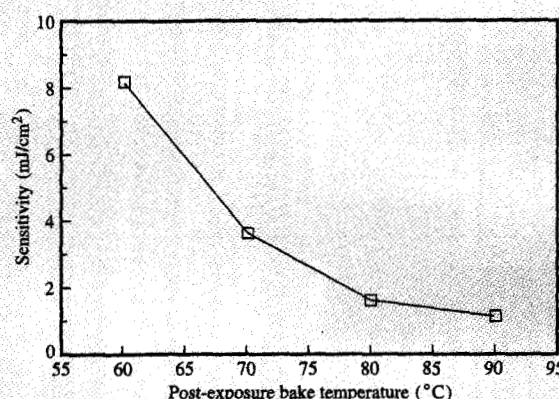


Figure 4

Change in resist sensitivity with post-exposure bake temperature for an early version of DUV resist, using tBOC resin.

observed for each subsequent batch of product wafers. This required "send-ahead" wafers to control image size for each lot, thereby significantly reducing throughput from the DUV sector (Figure 6).

While these difficulties rendered the process cumbersome, the development cycle of the 1Mb DRAM proceeded on schedule, and initial product demand was supplied. Several million fully functional 1Mb DRAM chips were produced with DUV (245-nm) technology.

In the laboratory, the negative-tone resist used on the 1Mb DRAM was shown to act as a positive-tone material if an appropriate polar developer was used [4]. In practice,

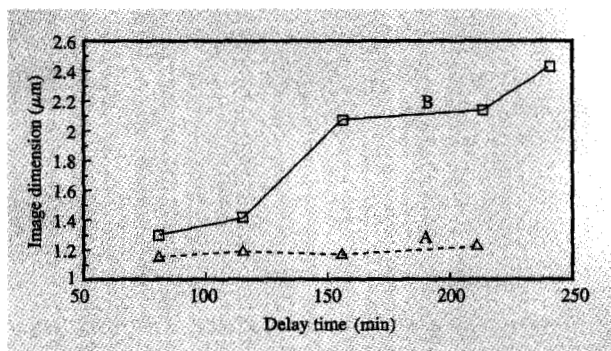


Figure 5

Plot of DUV resist sensitivity as a function of the delay time between baking of resist and resist exposure, with the wafers resting in a cassette on the photolithographic tool input station. Negative resist on wafers for 1Mb DRAM which have been "equilibrated" with contaminated fabrication facility air for a period of 2-3 hours became relatively stable to further change (Curve A), but required high doses (5 mJ/cm²) for image exposure. Wafers which had been processed through the resist application-bake steps immediately prior to processing in the photolithography tool (Curve B) were more sensitive (1.5 mJ/cm²) to exposure dose than the equilibrated wafers, but displayed rapid changes in sensitivity as they were allowed to interact with air in the fabrication facility.

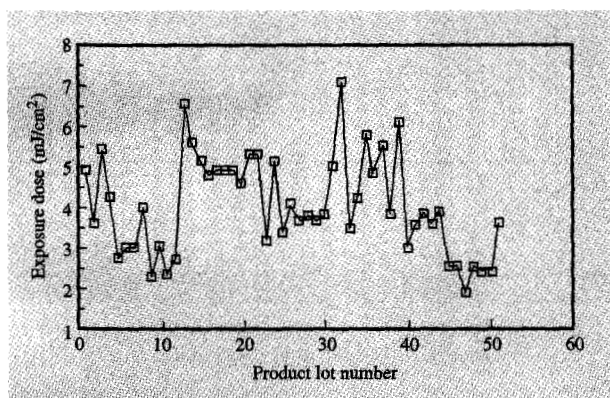


Figure 6

Exposure dose at $\lambda = 248$ nm as a function of product lot for negative DUV resist on a 1Mb DRAM Rox isolation mask level. Large changes in exposure dose between product lots were required to compensate for variations in the level of airborne contamination of each lot. Each lot was equilibrated with fabrication facility air for 2-3 hours prior to exposure.

the positive-tone image was distorted by an insoluble film at the surface of the exposed resist (Figure 7). After the experience with the negative-tone resist, it was realized that this inhibition effect was caused by chemical

contamination inadvertently poisoning the resist, and that a suitable positive-tone image could be formed if the effect of this contamination process was reduced or eliminated. When the resist was formulated to provide a higher dissolution rate of unexposed resist, the surface layer of contaminated resist could be removed in the development process, and a resist image with an acceptable profile was obtained.

As work on the 1Mb DRAM production shifted to more advanced G-line steppers (0.35 NA), the DUV effort was refocused on the 16Mb DRAM and the development of a positive-tone material which would overcome the limitations of this first-generation negative-tone DUV resist.

• 16Mb DRAM: Positive-tone DUV resist, 1987-1992

The experience gained from the 1Mb DRAM DUV development effort was used as a foundation for 16Mb DUV applications. When the 16Mb work began in 1987 at 500-nm resolution, conjecture centered on whether conventional optical lithography with single-layer resist processing would be attainable at the reduced depth-of-focus margins, or whether bilayer and top-surface imaging resists would be required [9]. At this time, I-line steppers were barely achieving the 0.7-μm resolution requirements of the 4Mb DRAM. A new DUV photolithography tool with a NA of 0.36 (discussed below in the section on photolithography tools) was developed which was suitable for 0.5-μm lithography. This tool was used for the 16Mb DRAM development program.

The 16Mb DRAM had six critical mask levels with resolution requirements of 0.5-0.6 μm and an overlay tolerance of 0.2 μm. Several of these levels contained critical features which were small openings (0.5-0.6 μm) printed in a field of resist. A positive-tone resist was desirable for these levels because of an enhanced focus window compared to negative-tone imaging and reduced reticle defects. (The positive-tone reticle was primarily a chrome area, which would mask particulates on the reticle surface, whereas a negative-tone reticle would have been mostly clear, allowing particles on the reticle to print as defects.) The negative-tone resist formulation used for the 1Mb DRAM was modified to create a positive-tone resist that overcame many of the initial DUV process control problems. The resin composition was modified to reduce loss of mass by decreasing the concentration of solubility inhibitor (which provided increased etch resistance and reduced image distortion) and to reduce the resist contrast. Reduced contrast allowed the resist to be more robust to chemical contamination by an airborne organic base. This, in turn, allowed aqueous-base developers to be used without adverse effects on the positive-tone resist profile. Resist chemical amplification was reduced by using

lower post-exposure bake temperatures and adding acid-quenching materials to the resist during formulation. While resist sensitivity was reduced by these changes, process latitude with respect to profile and sensitivity variations caused by unintended interruption of the chemical amplification process was increased. The use of aqueous-base developer allowed conventional HMDS surface treatments to be used for the enhancement of resist adhesion, thereby avoiding problems with lifting and cracking resist. Resin molecular weight was sharply reduced, which enhanced depth of focus and resulted in an absence of resist residuals after development. Nonmetallic photosensitizers were implemented, which further reduced residuals after resist-stripping processes. In addition, bottom antireflective coatings (ARC) and topcoat materials were developed to provide barriers to chemical contamination from both the wafer substrate and the processing atmosphere. As a result, the chemical amplification process in the resist could proceed without unintended interruption. These enhancements provided sufficient process stability for development and fabrication of the 16Mb critical mask levels. Since resist stability was sufficient, exposure dose could be controlled with statistical process control (SPC) charts rather than with send-ahead test wafers (Figure 8) [10]. The exposure dose was modified only if the average image size for a lot was outside the indicated control limits, or if seven lots in succession were above or below a target image size. The process steps for the first-generation positive-tone DUV resists are as follows:

- Adhesion prime or ARC apply/bake.
- Apply resist.
- Bake.
- Apply topcoat.
- Bake.
- Expose.
- Post-exposure bake.
- Develop in aqueous base.

SEM cross sections of selected features from the 16Mb DRAM critical mask levels are shown in Figures 9 and 10. The deep-trench storage capacitor (Figure 9) was printed with a resist opening $0.7\text{ }\mu\text{m}$ wide with a $0.5\text{-}\mu\text{m}$ separation between adjacent trenches. The isolation trench contained $0.5\text{-}\mu\text{m}$ resist lines with $0.6\text{-}\mu\text{m}$ spaces in the DRAM support structures. The surface strap, an electrical connection between the trench capacitor and the diffusion area, was printed as an $0.8\text{-}\mu\text{m}$ resist island with a $0.4\text{-}\mu\text{m}$ separation between adjacent straps. The straps were printed over the gate conductor topography, which was $0.8\text{ }\mu\text{m}$ in depth. The gate conductor (Figure 10) was a serpentine $0.6\text{-}\mu\text{m}$ line/space combination in the memory array, with $0.5\text{-}\mu\text{m}$ lines in the memory support features.

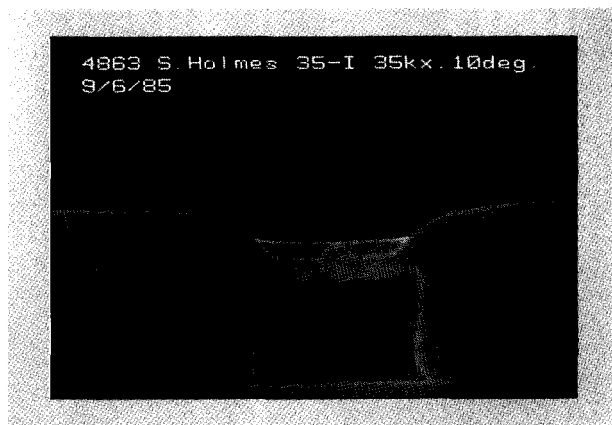


Figure 7

Cross section of resist for a contact hole imaged in a prototype version of DUV resist and developed with isopropyl alcohol. An insoluble layer present at the resist surface is caused by airborne chemicals in the processing area that interrupt the chemical amplification process near the resist surface.

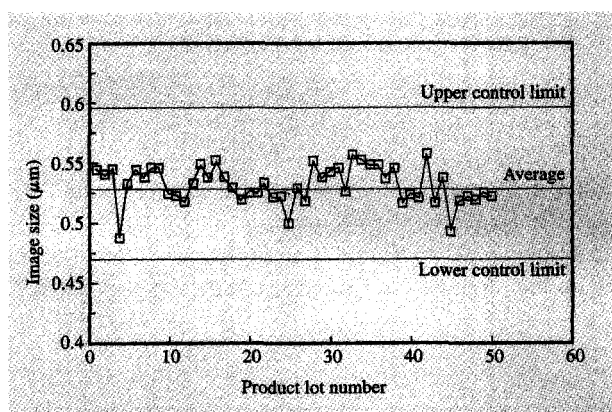


Figure 8

Statistical process control chart for the isolation trench (IT) feature of a 16Mb DRAM. Resist sensitivity and, consequently, image size are tightly controlled through the use of a resist topcoat material that prevents disruption of the catalytic image-formation process by contaminant chemicals in the fabrication facility air.

While the formulation changes for the 16Mb application of DUV resist relieved many of the initial problems, a continuing concern was the dependence of sensitivity on the post-exposure bake temperature (Figure 11). When more than one resist bake plate was used in a "clustered process," maintaining the temperature matching of the plates was often difficult. In a clustered process, the bake station is physically attached to the photolithography tool,

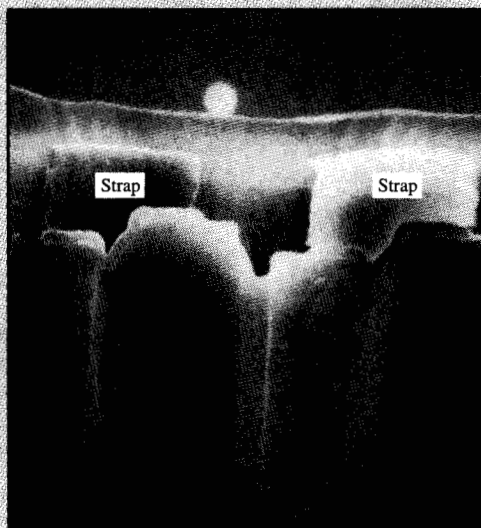


Figure 9

SEM cross section of deep-trench storage nodes in a 16Mb DRAM. Two polysilicon straps are shown, each connecting a diffusion to a deep-trench storage node. The trenches, $0.7\ \mu\text{m}$ wide and $8\text{--}9\ \mu\text{m}$ deep, are located between the vertical oxide collars. The structures were patterned with DUV resist at $\lambda = 245\ \text{nm}$.

and it is desirable to use a sufficient number of bake plates to match the throughput capability of the photolithography tool. In this arrangement, different bake plates are often used for successive wafers as they emerge

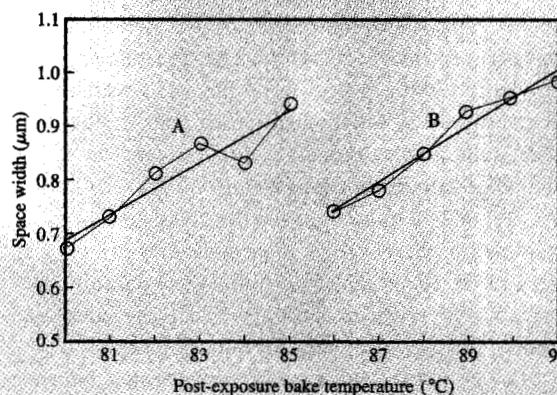
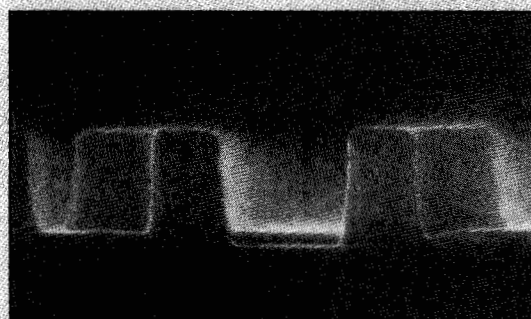


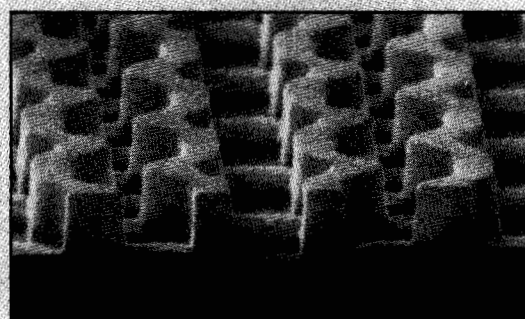
Figure 11

The width of spaces between positive-tone DUV resist images as a function of post-exposure bake (PEB) temperature for exposures at $19\ \text{mJ}/\text{cm}^2$ (Curve A) and $11\ \text{mJ}/\text{cm}^2$ (Curve B). Control of the post-exposure bake temperature was among the most critical parameters for control of image size.

from the photolithography tool. Gradual drift in bake-plate temperature could cause variation in wafer-to-wafer or lot-to-lot linewidth. Defects at the resist bake step, either from particles lodged between the wafer and the surface of the bake plate, or from failure of the positioning pins on the hot plate, could cause linewidth variation within a wafer. Prototype linewidth monitoring equipment was developed to monitor the image formation on a bake plate, both as a potential means of controlling



(a)



(b)

Figure 10

SEM cross sections of 16Mb DRAM gate conductor resist images with $0.6\text{-}\mu\text{m}$ linewidths, patterned with positive-tone DUV resist: (a) Cross section; (b) view of serpentine pattern.

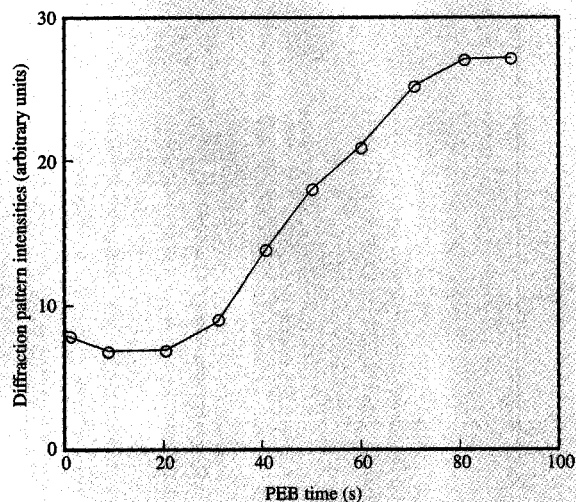


Figure 12

Example of an endpoint trace from an *in situ* monitor of the contact-via pattern image-formation process during the post-exposure bake. Intensities of diffraction patterns from the positive-tone DUV resist images were measured as a function of PEB time to derive a PEB endpoint.

the photolithographic-image size and as a means of detecting excursions in the bake process (**Figure 12**) [11], but are not implemented in manufacturing at present. The second-generation positive-tone DUV resist materials which are currently appearing in the marketplace provide more stability in the post-exposure bake process, as well as stability to airborne chemical contamination [12].

• *Logic gate conductor: 1992–1994*

During the characterization of the DUV positive-tone resist process, systematic within-chip differences in printing were observed. At the memory gate conductor level, in particular, isolated lines in the support areas were consistently wider than corresponding nested lines in a memory array. Because of the timing circuits which are present in the gate conductor features, this systematic difference caused yield reductions due to a loss in chip performance (**Figure 13**) [13(a)]. For the memory product, this linewidth deviation can be caused by both systematic etch and photolithography causes (**Figures 14 and 15**) [13(b)]. Polymer by-products of an etch plasma deposit more rapidly on the isolated features than the nested features, thereby causing the isolated lines to become wider than the nested lines [14]. The diffraction effects of the positive-tone aerial image caused the resist to print with a similar systematic bias, with isolated lines printing

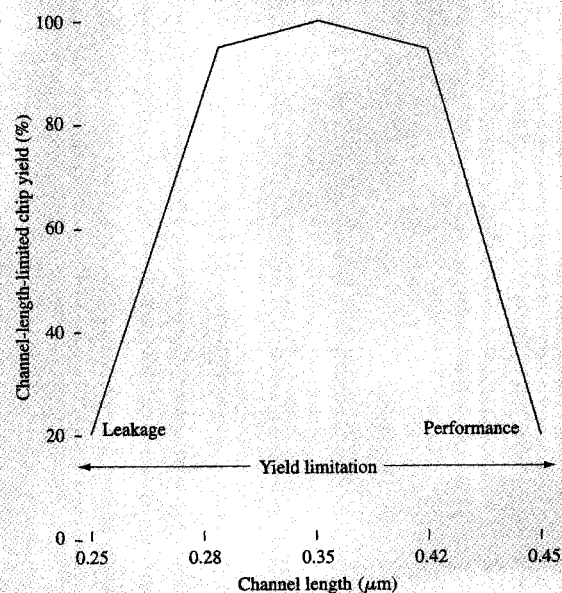


Figure 13

Schematic diagram of chip yield dependence on gate conductor channel length control. Channel length deviations to smaller feature sizes cause chip fails due to leakage, while excursions to larger feature sizes cause fails due to poor performance. (Reproduced from [13b], with permission.)

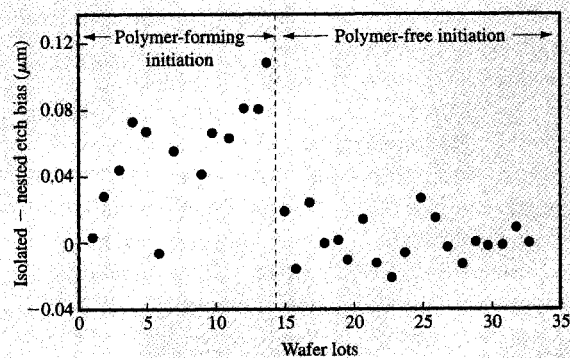


Figure 14

Within-chip image size deviations are caused by polymer-forming processes during gate conductor RIE image transfer. Lowering the levels of polymer formation by adjusting the etching process improved linewidth control and, consequently, resulted in higher chip yield.

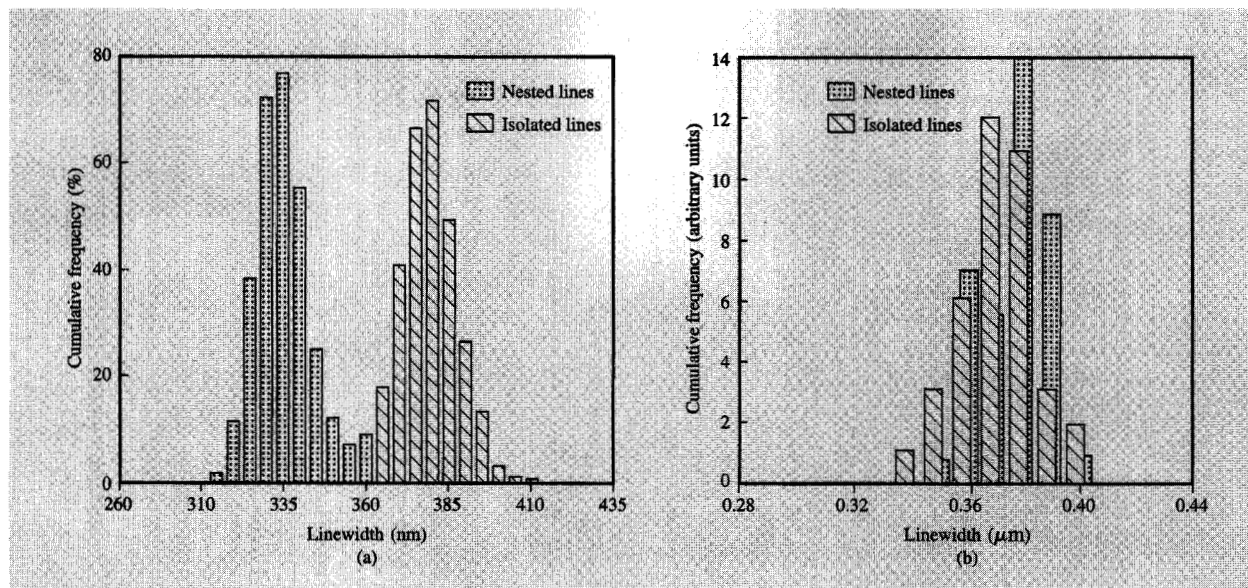


Figure 15

Within-chip 0.35- μm -linewidth image size deviations caused by diffraction effects in the aerial image using a 0.50-NA step-and-scan tool: (a) High-contrast, positive-tone resist exposed with diffraction-limited optics produces isolated lines which are systematically larger than nested lines, as illustrated by the two distinct measured linewidth distributions for this process. (b) Negative-tone patterning provides a narrower image size distribution for isolated and nested lines. (Reproduced from [13b], with permission.)

approximately 8% larger than nested lines. For the memory product, it was possible to optimize the reticle image size compensations to reduce this effect by using manual image inspection and compensation procedures. For logic applications, however, the irregular nature of the circuit pattern was too complex for manual alteration, and the features could not be automatically compensated with the available software technology.

The aerial image of negative-tone lines contains a minimal offset between nested and isolated lines [15]. In fact, the isolated lines print slightly smaller than the nested lines for negative-tone resist (Figure 15). This aids in compensating for the etch effect, which can be modified with etch chemistry and process, but which generally causes isolated lines to increase in width compared to nested lines for polysilicon etch processes (Figure 14).

A second-generation negative-tone resist was formulated to further enhance the DUV process capability [16]. This resist was used with a 0.5-NA step-and-scan exposure tool to achieve 0.35- μm gate conductor lithography. The mechanism of this resist is different from the initial DUV material in that the resin is cross-linked to impart insolubility to the exposed area. The previous resist had used a polarity change of the resin to impart insolubility to the exposed area. This new approach allowed a resist to be formulated which could be developed with an aqueous

base, providing the good adhesion characteristics obtainable with such systems. Cross-linking in this resist is very efficient, providing high-speed resist materials. As a result, chemical additives can be used to stabilize the resist to chemical amplification poisons without degrading the resist sensitivity or reducing wafer throughput. This negative-tone resist does not require a topcoat for process stability.

The cross-linking mechanism also provides a low-activation-energy image-formation process during the post-exposure bake. This results in a smaller variation of image size with post-exposure bake temperature, thereby further enhancing the manufacturability of DUV processes. Developer process latitude is also enhanced, since the image size for negative-tone resist is considerably more stable to develop time than for positive-tone resists.

The use of this resist, combined with enhanced etch processes and reticle uniformity, led to improvements in across-chip linewidth control for CMOS logic gate conductor programs. This enhanced linewidth control provides higher performance and yield values, which are the primary components for process manufacturing costs (Figure 16) [12, 13].

While the photoresists described were largely developed at IBM, an essential component in chip fabrication for device applications is the exposure tool used to image the

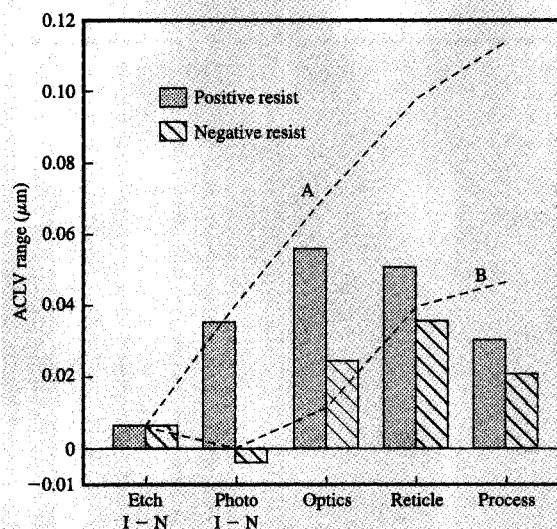


Figure 16

Across-chip linewidth variation (ACLV) of photolithographic and etch components: Curve A, positive-tone process (dotted columns) exposed with a 0.42-NA DUV step-and-repeat system; Curve B, negative-tone resist (shaded columns) exposed with a 0.50-NA DUV step-and-scan system. The positive-tone resist exposed with diffraction-limited optics produces isolated (I) lines which are systematically larger than nested (N) lines, as illustrated by the two distinct measured linewidth distributions for this process. Negative-tone patterning provides a narrower image size distribution for isolated and nested lines. While reticle fabrication continues to improve, it is a significant source of within-chip linewidth variation.

semiconductor patterns into the resist. During this application activity, IBM interacted closely with equipment suppliers to ensure that both the resist process and tool capabilities were commensurate with product requirements.

Evolution of DUV photolithography tool

• Prior to 1985

The first tool used for DUV manufacturing was a Perkin-Elmer full-wafer scanner (Table 1) with a curved-arc capillary mercury arc lamp source and reflective ring field projection optics (Figure 17). The reticle and wafer are mounted together on an air-bearing carriage which is scanned to image the entire wafer in a single pass. The tool achieves high wafer throughput in manufacturing because of the single scan per wafer.

The tool is adapted to DUV exposures using a filter in the illuminator/condenser. Since the illumination source is broadband and the reflective projection optics are corrected to less than 240 nm, resolutions of 1 μm needed

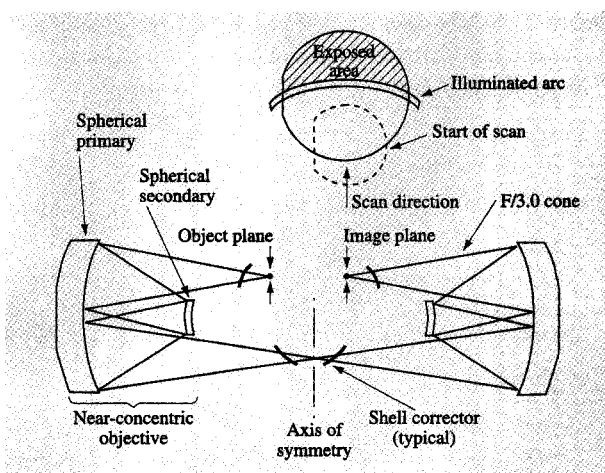


Figure 17

Schematic diagram of the projection optics for the first DUV scanning exposure tool, the PE-500, manufactured by the Perkin-Elmer Corporation. (With permission, SVG Lithography Systems, Inc., Wilton, CT.)

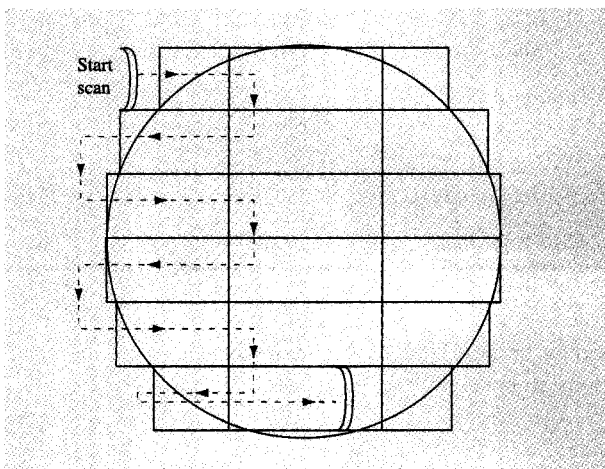


Figure 18

A stepping diagram for a step-and-scan exposure system. (With permission, [18].)

for 1Mb DRAM manufacturing could be achieved. This scanner was used in the 1Mb DRAM application described earlier.

The use of this tool at resolutions below 1 μm was not pursued because astigmatism was not fully corrected in some systems, and vertical and horizontal lines could differ by as much as 0.2 μm for a nominal 1.0-μm feature. Also, exposure uniformity was difficult to

Table 1 Comparison of attributes for a progression of DUV tools.

<i>Equipment principle</i>	Full wafer scanner	Step and scan	Step and repeat	Step and scan
<i>Supplier</i>	Perkin-Elmer	Perkin-Elmer/ SVG Lithography	Nikon	SVG Lithography
<i>Exposure source</i>	Mercury arc capillary lamp	Mercury-xenon arc lamp	KrF excimer laser	Mercury-xenon arc lamp
<i>Lamp power (kW)</i>	1	2.4	—	2.4
<i>Laser power</i>	—	—	3 W/200 Hz	—
<i>Bandwidth (nm)</i>	235–285	240–260	3 pm @ 248	244–252
<i>Uniformity (%)</i>	±3	±2	—	±1
<i>Projection optics</i>				
<i>Type</i>	Reflective	Catadioptric	Refractive	Catadioptric
<i>NA</i>	0.167	0.35	0.42	0.5
<i>Scanned field</i>				
<i>Shape</i>	Arc	Arc	Circle	Rectangle
<i>Height (mm)</i>	125	20.3	—	22
<i>Radius (mm)</i>	115	20	—	—
<i>Width (mm)</i>	4	1	—	5
<i>Printed field</i>	125-mm wafer	20 mm × 32.5 mm	15 mm × 15 mm	22 mm × 32.5 mm
<i>Stage</i>				
<i>Bearings</i>	Air	Air	Needle	Air
<i>Wafer (mm)</i>	125	200	200	200
<i>Alignment</i>	TTL	TTL	Off-axis	TTL
<i>Illumination</i>	Dark field	Reverse dark field	Dark field	Reverse dark field
<i>Distortion (nm)</i>	±250 (98%) (Dist & Mag)	±70	±120	±35
<i>Overlay</i>				
<i>Tool to tool (nm)</i>	350 (98%)	150 (98%)	150 ($x + 3\sigma$)	90 ($x + 3\sigma$)
<i>Ideal throughput</i>	100/hr	50/hr	24/hr	50/hr

achieve because the DUV illumination was not centered in the scanned slit.

• 1985 to 1992

As the 16Mb DRAM development program was initiated, there was a need for resolutions of 0.5 μm , the introduction of larger product chips, and the use of 200-mm wafers. This led IBM to acquire a tool from Perkin-Elmer designed specifically for DUV. This was the first tool (Table 1) based on the step-and-scan principle [17]. In tools of this type, the wafer is stepped to a new field, which is then scanned; this continues until all fields have been scanned (Figure 18).

Tools of the step-and-scan type are attractive for microlithography because they are able to print large fields at high wafer throughputs. Good resolution and low distortion can be obtained because the scanned field is small compared to the printed field and can be well corrected optically at higher NA values. Good linewidth control and overlay can be obtained because focus and

alignment can be adjusted during the scan of each field to match the topography and previous level pattern. With a bright illumination source, high throughput can be achieved because the stage can be scanned at high speeds.

The first step-and-scan tool from the Silicon Valley Group [18] required a 2.4-kW lamp and an arcuate light tunnel to provide a high-intensity uniform exposure dose at full scan speed. The 0.35-NA projection optics are of the reflective ring-field type with 4 $\times$ magnification capability added (Figure 19). In practical implementation, lenses are added for aberration correction. The alignment of the projection optics required a specially developed DUV interferometer to reach diffraction-limited performance.

A novel permanent magnet planar motor system and air-bearing wafer stage were developed to step and scan the wafer at velocities of 50 to 65 mm/s. The reticle and wafer stage were synchronized by master-slave servo control to ± 40 nm. Through-the-lens viewing was implemented at the 488-nm and 512-nm argon laser lines

to provide flexibility against thin-film interference effects. Active vibration isolation and temperature-controlled, chemically filtered air were provided to limit environmental influences on the projection optics and wafer.

This tool achieved a DOF greater than $\pm 0.75 \mu\text{m}$ at a resolution of $0.5 \mu\text{m}$. Full-field distortion was measured at $\leq 70 \text{ nm}$, and overlay capability on oxide wafers of 150 nm (98%) was achieved by using six-field global fine alignment. Product overlay performance for manufacturing tools of this type was 120 nm to 200 nm depending on the level. In production, the step-and-scan tool was capable of several hundred wafers per day and achieved reliability in excess of 200 hr mean time between fails (MTBF).

A 0.42-NA DUV Nikon stepper (Table 1) was also used for applications with ground rules of $0.5 \mu\text{m}$ or less. The all-quartz refractive lens of this tool required a $<3\text{-pm}$ -bandwidth excimer laser illumination source because of the single-material optical design. An advanced Cymer laser source was required for pulse-to-pulse stability and dose accuracy. The condenser optics relied on a fly's-eye lens and a vibrating mirror to achieve dose uniformity and low speckle. The condenser optics were pressurized slightly to prevent the accumulation of airborne contaminants on the lens surfaces.

This tool achieved a DOF of approximately $1.0 \mu\text{m}$ at a resolution of $0.45 \mu\text{m}$ and an overlay of $<150 \text{ nm}$ on product. The DUV stepper, which provided reliable production capacity, has a throughput of approximately two hundred wafers per day.

• 1993 to 1995

A 0.5-NA DUV step-and-scan tool (Table 1) was developed for resolutions of $0.35 \mu\text{m}$ and smaller [19]. The optics and development of the optional off-axis broadband viewing system represent significant changes from the original step-and-scan tool. A fly's-eye lens and light polarization are used to more than double the uniform exposure power to 20 mJ/cm^2 . The 5-mm-by-22-mm rectangular scanned field is produced using a compact beam-splitter cube design [19] (Figure 20). Through-the-lens viewing was improved and an off-axis viewing system added to provide viewing at higher NA with broadband illumination.

This tool achieves a DOF of $\pm 0.40 \mu\text{m}$ at a resolution of $0.35 \mu\text{m}$ and a full-field distortion that is significantly lower at $\leq 35 \text{ nm}$. Global fine alignment achieves an overlay of 90 nm on oxide films and a product overlay of 90 to 150 nm depending on the level.

• Beyond 1996

Step-and-scan tools equipped with a 0.6-NA lens for $0.25\text{-}\mu\text{m}$ resolution will soon be the standard DUV tool.

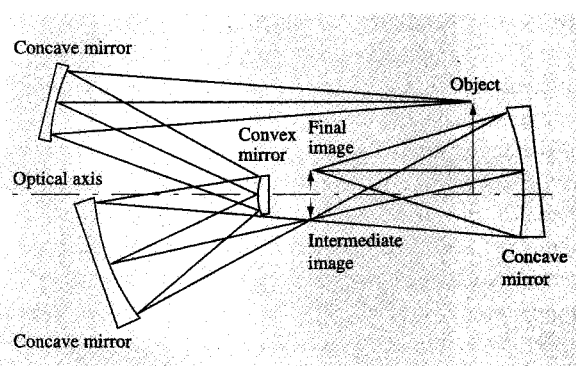


Figure 19

Schematic diagram for the projection optics of a 0.36-NA DUV step-and-scan exposure system.

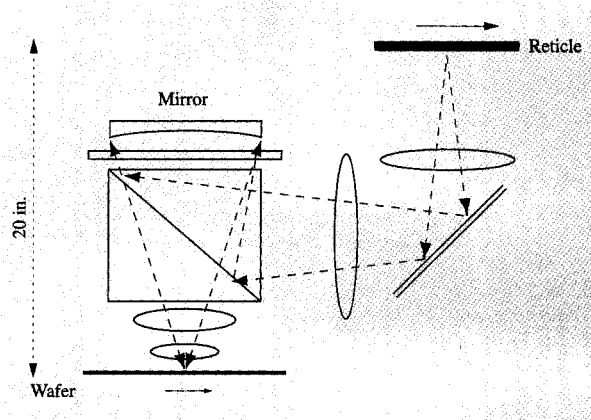


Figure 20

Schematic diagram for the projection optics of a 0.5-NA DUV step-and-scan exposure system. (With permission, [18].)

A high-repetition-rate excimer laser exposure source for these tools will provide enough power to expose less sensitive resists at higher stage speeds. The 0.6 NA will provide $0.25\text{-}\mu\text{m}$ images, but with a very small ($0.4\text{-}\mu\text{m}$) depth of focus. The use of off-axis illumination and variable σ should partially alleviate the depth-of-focus limitations. Overlay will be improved because optical distortions become smaller, and better viewing and stage capabilities will be available. Wafer throughputs and productivity will improve because the stages are being driven faster.

Lithography outlook: 1996–2000

Optical lithography continues to push beyond the anticipated limits, as state-of-the-art I-line production approaches 0.35- μm features and as high-NA DUV tools achieve sub-0.25- μm capability [20]. DUV resist performance will continue to improve as diffusion effects related to the chemical amplification process are minimized and resin dissolution characteristics are enhanced. Circuit designs compatible with off-axis illumination, combined with the availability of phase-shift reticle inspection and repair equipment, will further extend the capability of optical lithography. Scaling the exposure wavelength an additional 20% with 193-nm systems [21], combined with these other techniques, should provide a path to a sub-0.15- μm lithography capability.

Acknowledgments

The authors gratefully acknowledge Grant Willson, Hiroshi Ito, Nick Clecak, Russ Wendt, Clint Snyder, Bill Brunsvold, Will Conley, Rob Wood, George Hefferson, Karey Holland, Al Bergendahl, John Sturtevant, Paul Rabidoux, Denis Poley, K. C. Norris, Steve Lapine, Curt Rude, Roger Barr, Bob Cogley, Bob Batterson, Mike Charney, and Hal Linde.

References

1. J. D. Buckley, "Expanding the Horizons of Optical Projection Lithography," *Solid State Technol.* **25**, 77–82 (May 1982).
2. M. Hakey and W. Straub, "Advanced 1X Projection Lithography," *J. Electron. Mater.* **11**, 813–830 (1982).
3. (a) H. Ito and C. G. Willson, *Polym. Eng. Sci.* **23**, 1012–1018 (1983). (b) H. Ito and C. G. Willson, in *Polymers and Electronics*, ACS Symposium Series, No. 242, T. Davidson, Ed., American Chemical Society, Washington, DC, 1984, pp. 11–23. (c) H. Ito, J. Frechet, and C. G. Willson, "Positive- and Negative-Working Resist Compositions with Acid Generating Photoinitiator and Polymer with Acid Labile Groups Pendant from Polymer Backbone," U.S. Patent 4,491,628, 1985.
4. H. Ito, "Chemical Amplification Resists: History and Development Within IBM," *IBM J. Res. Develop.* **41**, 69–80 (1997, this issue).
5. J. Maltabes, S. Holmes, J. Morrow, R. Barr, M. Hakey, G. Reynolds, W. Brunsvold, C. G. Willson, N. Clecak, S. MacDonald, and H. Ito, "1X Deep UV Lithography with Chemical Amplification for 1-Mbit DRAM Production," *Proc. SPIE* **1262**, 2–7 (1990).
6. H. Ito, "Chemically Amplified Resists—History and Recent Progress," *Proceedings of the 10th International Conference on Photopolymers*, Mid-Hudson Section, Society of Plastics Engineers, 1994, pp. 1–11.
7. J. Sturtevant, S. Holmes, and P. Rabidoux, "Post-Exposure Bake Characteristics of a Chemically Amplified Deep-Ultraviolet Resist," *Proc. SPIE* **1672**, 114–124 (1992).
8. S. MacDonald, N. Clecak, R. Wendt, C. G. Willson, C. Snyder, C. Knors, N. Deyoe, J. Maltabes, J. Morrow, A. McGuire, and S. Holmes, "Airborne Chemical Contamination of a Chemically Amplified Resist," *Proc. SPIE* **1466**, 2–12 (1991).
9. D. E. Seeger, D. C. La Tulipe, Jr., R. R. Kunz, C. M. Garza, and M. A. Hanratty, "Thin-Film Imaging: Past, Present, Prognosis," *IBM J. Res. Develop.* **41**, 105–118 (1997, this issue).
10. (a) S. Holmes, R. Levy, A. Bergendahl, K. Holland, J. Maltabes, S. Knight, K. C. Norris, and D. Poley, "Deep Ultraviolet Lithography for 500-nm Devices," *Proc. SPIE* **1264**, 61 (1990). (b) S. Holmes, A. Bergendahl, D. Dunn, M. Hakey, K. Holland, D. Humphrey, S. Knight, D. Poley, P. Rabidoux, K. C. Norris, J. Sturtevant, and D. Writer, "Deep UV Lithography for the Manufacture of 16-Mb DRAM Devices," *Proc. SPIE* **1671**, 57 (1992). (c) J. Sturtevant and S. Holmes, "Deep-UV Lithography in 16-Mbit DRAM Manufacturing," *Micro lithography World*, pp. 17–22 (August 1993).
11. J. Sturtevant, S. Holmes, T. Van Kessel, P. Hobbs, J. Shaw, and R. Jackson, "Post Exposure Bake as a Process Control Parameter for Chemically Amplified Photoresist," *Proc. SPIE* **1926** (1993).
12. W.-S. Huang, R. Kwong, A. Katnani, M. Khojasteh, and K. Lee, "An Environmentally Robust Positive Tone Chemically Amplified Resist—KRS," *Proceedings of the 10th International Conference on Photopolymers*, Mid-Hudson Section, Society of Plastics Engineers, 1994, pp. 96–106.
13. (a) S. Holmes, D. Sundling, J. Adkisson, J. Sturtevant, M. Hakey, D. Horak, W. Conley, and A. Katnani, "Gate Conductor Lithography for 350-nm Devices," *Proceedings of the 10th International Conference on Photopolymers*, Mid-Hudson Section, Society of Plastics Engineers, 1994, pp. 396–405. (b) S. Holmes, M. Hakey, J. Sturtevant, and D. Dunn, "Overview of DUV Lithography for 350-nm CMOS Device Fabrication," *Proceedings, Semicon/Kansai-Kyoto '93 Technology Seminar*, 1993, pp. 85–96.
14. D. G. Chesebro, J. W. Adkisson, L. R. Clark, S. N. Eslinger, M. A. Faucher, S. J. Holmes, R. P. Mallette, E. J. Nowak, E. W. Sengle, S. H. Voldman, and T. W. Weeks, "Overview of Gate Linewidth Control in the Manufacture of CMOS Logic Chips," *IBM J. Res. Develop.* **39**, 189–200 (1995).
15. C. A. Mack and J. E. Connors, "Fundamental Differences Between Positive and Negative Tone Imaging," *Proc. SPIE* **1674**, 328 (1992).
16. (a) W. Conley, R. Sooriyakumaran, J. Gelorme, S. Holmes, M. Petryniak, R. Ferguson, R. Martino, P. Rabidoux, and J. Sturtevant, "Negative Tone Deep-UV Resist for 16-Mb DRAM Production and Future Generations," *Proc. SPIE* **1925**, 11 (1993). (b) W. R. Brunsvold, W. E. Conley, J. D. Gelorme, R. Nunes, R. Sooriyakumaran, S. J. Holmes, and J. L. Sturtevant, "Further Improvements in CGR Formulation and Process," *Proc. SPIE* **2195**, 329–340 (1994).
17. D. A. Markle, "The Future and Potential of Optical Scanning Systems," *Solid State Technol.* **27**, 165 (1984).
18. C. Karatzas and J. D. Buckley, "Step-and-Scan: A Systems Overview of a New Lithography Tool," *Proc. SPIE* **1088**, 424–433 (1989).
19. H. Sewell, "Step-and-Scan: The Maturing Technology," *Proc. SPIE* **2440**, 49–60 (1995).
20. M. D. Levenson, P. J. Silverman, R. George, S. Wittekoek, P. Ware, C. Sparkes, L. Thompson, P. Bischoff, A. Dickinson, and J. Shamaly, "Welcome to the DUV Revolution," *Solid State Technol.* **38**, 81–98 (1995).
21. M. Hibbs, R. Kunz, and M. Rothschild, "193-nm Lithography at MIT Lincoln Lab," *Solid State Technol.* **38**, 69–78 (1995).

Received February 9, 1996; accepted for publication December 2, 1996

Steven J. Holmes *IBM Microelectronics Division, Burlington facility, Essex Junction, Vermont 05452 (SHOLMES at BTVLABVM, sholmes@vnet.ibm.com).* Dr. Holmes is a photolithography development engineer in the Emerging Technologies Department. He received a B.S. in chemistry from Yale University in 1979, and a Ph.D. in chemistry from M.I.T. in 1983. After postdoctoral studies at Purdue in organic chemical synthesis, he joined IBM at its Essex Junction, Vermont, semiconductor development facility. Dr. Holmes has worked on DUV resist and applications development since that time, with projects including 1Mb and 16Mb DRAM development, logic gate conductor and logic local interconnect lithography. He is currently working on lithography development for sub-quarter-micron logic and memory applications.

Peter H. Mitchell *IBM Microelectronics Division, Burlington facility, Essex Junction, Vermont 05452 (PMITCHEL at BTVMANVM, p_mitchell@vnet.ibm.com).* Mr. Mitchell joined IBM in 1968 at the Microelectronics Division semiconductor manufacturing facility in Essex Junction, Vermont. He holds B.S. and M.S. degrees in electrical engineering from Cornell University and a professional degree in electrical engineering from Massachusetts Institute of Technology (MIT). Mr. Mitchell has worked with DUV exposure equipment for the past ten years. Prior to that he worked with hot process equipment and computer monitoring and control of semiconductor manufacturing equipment.

Mark C. Hakey *IBM Microelectronics Division, Burlington facility, Essex Junction, Vermont 05452 (mhakey@vnet.ibm.com).* Mr. Hakey received his undergraduate degree in chemistry from St. Michael's College in Winooski, Vermont, in 1972 and attended graduate school at the University of Vermont, also in chemistry, from 1972 to 1974. Subsequently, he joined Union Carbide Corporation, where he worked for five years on electroplating and injection molding processes. In 1978 Mr. Hakey joined IBM, where he was originally involved in lithography process development for G-line systems. He subsequently worked in I-line and DUV systems and tools, later managing lithography and etching groups. In the mid-1980s, he worked on teams qualifying 1Mb DRAM chips for IBM, and in the late 1980s and early 1990s managed the technology development team for 16Mb era memory and logic products. Technology innovation implemented into manufacturing included DUV lithography on step-and-scan systems, positive and negative DUV resist systems, shallow trench isolation, and ultrahigh-aspect-ratio DRAM storage node trenches. Since 1994, Mr. Hakey has managed the Emerging Technologies Department based in the Advanced Semiconductor Research Center and in Burlington, Vermont.